CFO TRACKING FOR DIRECT RF SAMPLING ARCHITECTURE APPLIED TO VHF AVIONIC RADIOS

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Abstract
Recently, many efforts have been made to respond to the increasing demands of a new RF avionic generation, in which Direct RF Sampling (DRFS) has been considered as a promising solution to satisfy the Size, Weight, Power and Cost (SWaP-C) constraints. In this architecture, Direct Digital Synthesizer (DDS) plays a key role, significantly affecting the overall performance of the whole system. Theoretically, the output of DDS should have alias frequency of the Signal of Interest (SOI) in the first Nyquist zone. However, due to the resolution of the tuning word and the difference in frequency of the transmitter from the assigned frequency, this signal might differ from the target carrier, resulting in an inaccuracy shift of the digital mixer. Furthermore, this issue will distort the output signal and deteriorate the performance of the receiver. The work presented in this paper introduces an approach to solve this problem. Based on the conventional Automatic Frequency Control (AFC), the configurable Fast Fourier Transformation (FFT) based Carrier Frequency Offset (CFO) Tracking System has been designed and implemented to meet the new challenges of DRFS in avionic receiver design. The experimental results show that the integration of this module increases the sensitivity of the DRFS architecture for avionic applications, such as VHF Omnidirectional Range (VOR), Instrument Landing System (ILS) and VHF audio communication.

Introduction
With the development of aerospace engineering, there has been an increasing demand for a new generation of avionic systems, attracting the interests of researchers and industries for years. The requirements for the next generation of the avionics are minimizing and simplifying the integrated components, meanwhile increasing their security and accuracy. In current years, with the appearance of wideband Analog to Digital Converters (ADC), which support the sampling rate of hundreds of MHz to GHz, new solutions have been introduced. In 2012, G. Lamontagne et al [1] proposed a DRFS architecture for GNSS, which is compatible with GPS and GLONASS signals. As mentioned in their conclusions, by using an ADC with the sampling rate of 300 MHz, without any Local Oscillator (LO) Mixer, the DRFS architecture has similar performance to the current commercial devices. In 2015, O. A. Yeste-Ojeda et al [2] studied the application of DRFS in VHF RF avionics, aiming at VOR, ILS, Aircraft Communication Addressing and Reporting System (ACARS), etc. Based on their proposed architecture, which uses an ADC directly after the receiving antenna, as shown in Figure 1, there is no need for analog components in Intermediate Frequency (IF) stages. By replacing the LO mixer by a digital mixer after the ADC, this approach reduces unwanted effects such as LO leakage, DC offsets, IQ imbalance, etc. In addition, this architecture is suitable for implementing a multi-standard avionic receiver. In other words, with this approach, the goal of combining Communication, Navigation and Surveillance SOIs in modern avionics can be done with just one ADC and one Central Processing Unit (CPU).

Figure 1. General Front-End DRFS Architecture

Generally, in the digital domain, there are two methods to down-convert the SOI into baseband. The first and more popular one is using digital mixers. Figure 2 shows a simple implementation of this
module, which is a combination of a DDS to create the required signal and a multiplication. The second approach uses CORDIC rotation, as presented in [3].

**Figure 2. Digital Mixer Using DDS**

In either way, the main point is that the output after the down-converter should be the SOI in baseband, filtered any out-of-band tone, and has a suitable sampling rate for any processing downstream. The principle of this digital mixer applied for DRFS is described in Figure 3. With the digital mixer, the quality of the outputs, whether they are numbers (in the case of navigation systems) or data (in other cases), depends strongly on the accuracy of the signal created by the DDS. A small difference in frequency between the SOI and the generated signal will cause a shift in baseband, deteriorating the general performance of the system.

**Figure 3. Principle of Digital Mixer in DRFS**

Table 1 summarizes the component signals, the required sensitivity as well as the tolerance in the frequency of the SOIs.

**Table 1. Standards of the SOIs [5] – [7]**

<table>
<thead>
<tr>
<th>Offset</th>
<th>Tones</th>
<th>Spacing</th>
<th>Sensitivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOR  ±1.2 kHz</td>
<td>30 Hz, 1020 Hz, 9960 Hz, AM</td>
<td>50 kHz</td>
<td>-93 dBm</td>
</tr>
<tr>
<td>LOC ±9 kHz</td>
<td>30 Hz, 150 Hz, 1020 Hz, AM</td>
<td>50 kHz</td>
<td>-87 dBm</td>
</tr>
<tr>
<td>GS ±17 kHz</td>
<td>30 Hz, 150 Hz, AM</td>
<td>50 kHz</td>
<td>-78 dBm</td>
</tr>
<tr>
<td>VHF radio ±4 kHz</td>
<td>Voice, AM</td>
<td>50 kHz</td>
<td>-105 dBm</td>
</tr>
</tbody>
</table>

The tuning problems have been recognized for a long time, along with the solutions for conventional
RF receivers. Referring as “inaccuracies manual tuning and oscillator drift”, C. Travis presented a system called AFC to solve this problem [4]. The mechanism of this system is simple but efficient, as it will continuously adjust the output of the LO based on the detected bias by a frequency sensitive detector. To reduce the pressure in RF design and the separation space between channels, receivers need higher selectivity and more precise AFCs. These systems might vary depending on the architecture (heterodyne, zero-IF, superheterodyne, etc.) and the applications. For example, in the case of a Direct-Conversion architecture, A. R. Behzad et al [8] presented a transceiver design and implementation for 5 GHz IEEE 802.11a Wireless LAN standard, using AFC to track the frequency offset of Orthogonal Frequency Division Multiplexing (OFDM) signals. Because of the tolerant standards for this offset, a hybrid mechanism (analog and digital) was implemented. In this kind of AFC, the digital parts will be in charge of calculation the offset in frequency, making adjustments if necessary and directly controlling the function of the analog components. In the last few decades, great efforts have been devoted to developing the algorithms for this frequency estimation, which concentrated on saving computational resources. These algorithms can be divided into two groups. One is based on FFT, in which some well-known candidates are FFT-based No Post-Processing, FFT-based Newton’s Method, FFT-based Quadratic Interpolation, etc. The other group is Linear-Regression-Based, offering the advantages of computational simplification and less latency. A summary of the benefits and drawbacks of these algorithms can be found in [9].

Since there is no LO mixer in DRFS architecture, the conventional hybrid approaches cannot be implemented. In this paper, a solution for this problem is presented, which is directly modifying the bits of the tuning word fed to the DDS in the digital domain. The designed AFC is implemented regarding the following conditions:

- Like most of the avionic signals, these SOIs are Amplitude Modulation signals, as it is more efficient in spectrum separations and it can reduce the unnecessary cost to integrate new modulation technique [10].
- The acceptable tolerance for each of the SOIs is different, with the highest value of 17 kHz for GS.
- All of the SOIs are continuous signals or last at least few seconds, which lowers the requirement for latency. In terms of ground station transmitter, the shift from the assigned frequency and the real carrier are fixed, meaning that the estimator only needs to run few times to lock the carrier of the SOI.
- Since the AFC is just a small module in the receiver architecture, it should be integrated with a trade-off among resource utilization, complexity, and accuracy.

This paper proposes a mechanism compatible with the DRFS architecture, and more importantly, which can adapt itself to the characteristics of the SOIs. By using FFT and Max Hold to find the frequency with the highest magnitude, the proposed FFT based AFC can be implemented by fully digital modules and integrated directly in the FPGA, which does not require any supporting analog components. The results of laboratory tests show that the proposed system can function properly with inputs as low as -110 dBm, which is better than the standards presented in Table 1. In addition, the functionality of these modules is controllable and can be activated/deactivated in runtime, making it possible to build a more flexible system in the real working environment.

In the next section of this paper, an overview of the proposed FFT based AFC and its implementation in FPGA level is presented. Then, to validate the proposed mechanism, the results of the laboratory experiments with certified avionic testing equipment (Aeroflex IFR-4000) are presented and analyzed. These analyses are explained in two parts, the first part focuses on the general performance of the AFC, particularly in the sensitivity, robustness, and resource utilization. The second part, which is the main one, discusses the effect of the proposed modules on the performance of the developed DRFS architecture, focusing on VOR, ILS and VHF audio systems. The last section provides the conclusion of this paper, as well as the perspective for future research.
Configurable FFT Based AFC

Architecture and Design

To solve the issues of the DRFS architecture and based on the characteristics of the SOIs, FFT-based Automatic Frequency Estimator using Maximum Power Estimation is the chosen solution. In spite of the problem at the low level of SNR, as mentioned in [6], the standards of the SOI showed in Table 1 assure that the proposed AFC will never have to work in these negative SNR cases. In order to save FPGA space, a single AFC system is integrated for all four applications, running in parallel with the main DDC/DUC architecture. This module is controlled and configured by an integrated control mechanism, of which the operation can be divided into two steps:

- **Coarse correction**: Manually assigning a frequency to each system. The maximum shift after this stage will not be higher than ±18 kHz.

- **Fine correction**: Adjusting the tuning word from the first correction with the FFT result. The frequency resolution of the proposed AFC, as well as resource utilization and latency, will be determined by the length of the FFT.

Figure 5 presents the block diagram of the proposed AFC regarding the main systems. In general, this system is divided into five modules, namely Controller, Digital Down Converter (DDC), FFT Calculation, Max Hold and Tuning Word Corrector. The reconfigurability of the proposed AFC is based on the Controller Module, which is, in fact, a 10-bit word manipulated by an operator, as described in Figure 6. The first two bits are used to switch between SOI and control the input flow of the DDC. After calculation, the next four bits decide whether to remember the modified word of each channel or not. Finally, the four most significant bits control which word is fed into the main system.

![FFT based AFC module](image)

**Main DDC system**

![Digital Down Converter](image)

Figure 5. Integration of the Frequency Control
Figure 6. Implementation of the Control Unit

It is clear that after the coarse correction, the AFCs only need to find the SOI in a maximum bandwidth of 35 kHz. Furthermore, the sampling rate for the FFT calculation process should be decimated from the original one after the ADC. This is the operation of the DDC module, which in other words is the structure of decimation filters. In digital signal processing, there are two mainstream digital filter architectures, Finite Impulse Response (FIR) and Infinite Impulse Response (IIR). While the first has the advantages of simplicity in design and implementation, as well as fully supported in FPGA with various pre-designed IP cores, the latter offers the possibility of saving FPGA resources and less latency [11], [12]. Nevertheless, with the sampling rate of 200 kHz, after the DDC, IIR structure is not easily achievable, because it might violate the timing constraint; hence, it should be pipelined [12]. In the scope of this work, both FIR and IIR structures are implemented and investigated in the DDC sub-module to have an overview of the effects related to these filters on the main FPGA functionalities, particularly in latency and resource. The results of these integrations are presented in the next section. Based on this data, the structure with better performance will be integrated into the final architecture of the proposed system.

After down-conversion, I and Q of the un-optimized tuning word are fed into the FFT with the length of L. The complex output of this calculation will pass a multiplication and then an addition to have an easy estimation of magnitude. Next, all of these values pass through a Max Hold module, saving and outputting the corresponding index in the range of \([1, L/2]\) with maximum magnitude. Then this fine correction value is added to the coarse entered tuning word and the final corrected one can be obtained.

Implementation in FPGA

In this work, the Nutaq PicoDigitizer250 is used as the SDR component. The ADS62P49 in the motherboard offers a sampling rate up to 250 MSPS, with 14 bits resolution. In implementation, the clock rate of the ADC is set to 140 MSPS [2], providing a 70 MHz bandwidth in the first Nyquist zone according to DRFS theory. This bandwidth is more than enough for the selected applications while avoiding any collapse between systems. FPGA is developed with Xilinx System Generator. The DDS is implemented with Spurious Free Dynamic Range (SFDR) at 96 dB, resolution at 0.05 Hz and Noise Shaping with Phase Dithering. These settings need a 32 bits input tuning word [13]. In order to adapt the system with the tolerance mentioned in the RTCA documents (Table 1), the proposed AFC should track both positive and negative offset frequencies from the input value. Therefore, the tuning word of the AFC is shifted 18 kHz to left. Thus, the maximum amplitude position is always on the positive side after the DDC. Because of the shift, the cut-off frequency of the filters has to be at least twice the maximum tolerance of all systems.

Figure 7 and Figure 8 show the architecture of the DDC (CIC/FIR filters) and the Max Hold module, respectively, integrated into the proposed AFC. To reduce the order of the FIR filter, CIC filters are used to do the decimation before passing the data to the FIR. As a result, the FIR sampling rate is only 200 KSPS. This rate is enough to make sure that a 146-order FIR is enough to have a suitable magnitude response. In terms of IIR filters, the design process is more complicated. The rate of 200 KSPS is not suitable for a structure with feedback as in IIR; therefore, extra pipelining has to be done. Due to its stability, Cluster Look-Ahead (CLA) method is chosen [12], [14]. The final result of this implementation is a 4-section, 6-order IIR filter structure. Figure 9 shows the differences of an IIR section before and after pipelining, where Ni and Di are Numerators and Denominators respectively.

2D3-5
In order to compare the differences in latency between two filter structures, the following experiment is performed. The ADC of the PicoDigitizer is wired directly to a Signal Generator, which is set to create an AM signal at 331.72 MHz, with modulation depth of 50% and 1020 Hz tone. The behavior inside FPGA is observed and saved using ChipScope Pro Analyzer, where the trigger is the corrected tuning word (0101 1110 1001 0101 0000 0001 0100 1111). At the beginning, the frequency is set at 331.78 MHz in GNU Radio, and there was no trigger. After setting this value to 331.71 MHz, the FFT found the corrected tuning word using the output of the DDC, as described in Figure 10 and Figure 11, respectively.
Figure 11. FIR (red) and IIR (blue) Results

It can be seen that it is the FIR structure which triggered the correct word (marked by O) 30 samples before IIR structure gets that value (marked by X). Since the implementations of both structures are the same, except the FIR and IIR, it can be concluded that the only reason for this difference is the filter. With the sample rate of 200 KSPS, the latency of IIR filter is 150 µs greater than FIR filter. Since this difference in latency is still the same regarding the level of input signal, from -30 dBm to -110 dBm, it is clear that after pipelining, the IIR structure has lower performance than the FIR.

Table 2 describes the resource utilization of the designed FPGA before and after integrating the proposed AFC, with both FIR and IIR filters. The percentages are obtained from Xilinx Project Navigator, regarding the available resources in Virtex6-xc6vsx315t FPGA. The first considerable point from Table 2 is that the proposed AFC consumes only a small amount of the available resources. In fact, except RAM/FIFO (it is essential for doing the multiplications and addition of FFT), all the other categories increase less than 5%. Although these numbers might vary depending on the Q factor of the filters or length of the FFT, it can be concluded that the proposed AFC has no significant requirements for calculating resources. The second point is the differences between FIR and IIR implementation. Even though, theoretically, the IIR filter offers the possibility of resource saving, in reality, pipelining increases the number of registers and Look-Up Table (LUT) components, so consequently it ends up using more resources. Since FIR structure has the advantages in both parameters (latency and resource utilization), it can be chosen to implement the full system. From this point, all of the results in this work will be only related to the AFC using FIR filters in DDC.

Table 2. Resource Utilization of the AFC

<table>
<thead>
<tr>
<th>Slice Logic Utilization</th>
<th>Original</th>
<th>AFC (FIR)</th>
<th>AFC (IIR)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slice register</td>
<td>13%</td>
<td>16%</td>
<td>17%</td>
</tr>
<tr>
<td>Slice LUTs</td>
<td>20%</td>
<td>24%</td>
<td>28%</td>
</tr>
<tr>
<td>Memory</td>
<td>10%</td>
<td>12%</td>
<td>13%</td>
</tr>
<tr>
<td>Fully used LUT Flip Flop</td>
<td>51%</td>
<td>54%</td>
<td>52%</td>
</tr>
<tr>
<td>RAM/FIFO</td>
<td>41%</td>
<td>52%</td>
<td>52%</td>
</tr>
</tbody>
</table>

The most important sub-component in this proposed system is the FFT module, which is a supported IP core in System Generator. The required resources for this core varies according to the settings (scaled, unscaled, Radix2, Multiplier, etc.) and most importantly, the length L. The length is proportional to the final resolution of the AFC, as well as the latency and the computational complexity [15]. Based on the standards of the SOIs in Table I, L is set at 32768. As a result, the resolution of the AFC is around 3Hz. With this setting, the worse latency from the time when the first input is fed into the FFT core to the time that the Max Hold determines the index is around 1.5-2 times L, which is almost 250 - 330 ms.

Results and Analysis

**General Performance**

Figure 12 shows the shift problem created by rounding and quantization of the tuning word. Both TX and RX signals have been set at 108 MHz, however, at downstream in GNU Radio, the FFT of the output shows that the carrier is not centered. This shift results in a close-to-DC frequency, distorting the AM signal. Then this wrong tuning word is modified by the AFC, improving the results, as can be seen in Figure 13. The outputs still have a shift of 0.5 – 1 Hz,
since the resolution of the FFT is 3 Hz, however, the signal is now steady enough for further calculation.

Figure 12. Offset in Frequency Issue

Figure 13. The Results after Correction

After testing with various signals at different levels, the results show that the proposed AFC have good performance in case of AM signals. It can track and lock any AM signal at a range of ±18 kHz from the input frequency, ranging from above -25 dBm to below -100 dBm. However, they show inaccuracy for FM signals which can be explained as the nature of two modulations. In terms of AM, it is easy to determine the center peak of the carrier, which is impossible for FM. Since AM is the main modulation applied to avionic signals [10], this limitation would not be a major drawback of the proposed AFC.

When we have multiple input frequencies, the filters in DDC will attenuate the out-of-band signals, helping the Max Hold to locate correctly the index. In order to evaluate the robustness of the AFC against interferences, the SDR is connected with both an IFR-4000 and a Signal Generator. The IFR-4000 is set at LOC mode, 108.1 MHz, with the output levels of -30, -60 and -90 dBm. While, the output of the Generator is an AM signal, with the rate of 1 kHz, depth of 50%, with variable frequencies and levels. The maximum level of the Generator at which the AFC failed to track the SOI is noted for each spacing. Since the maximum input level mentioned in the standards for all of the SOIs is -25 dBm [2], the maximum level of the interference in this experiment is also set to this value. Figure 14 shows that, above the bandwidth of the integrated filter in DDC, the interferences are attenuated almost 40 dB at ±20 kHz. Besides, the AFC ignores any interference with spacing outside of ±25 kHz, the minimum channel among the SOIs.

Figure 14. AFC Robustness Analysis

Impact on the Performance of Avionic Systems

VOR

In this test, the IFR-4000 is connected directly to the PicoDigitizer. The signal is set at 108 MHz, 210 degrees of bearing, at -80 dBm. Figure 15 demonstrates the calculated bearing before (the first half) and after (the second half) correcting the tuning word with AFC. It is clear that without correction, the results could not meet the acceptable error rate (< ±3 degrees at 95%). In contrast, after correction, the outputs are correct and stable. Figure 16 displays the accuracy of the system with different input levels, using different tuning words. As it can be seen, the AFC increases the sensitivity of the VOR by at least 20 dB in case of no correction, and 3 dB in case of manual tuning of frequency.
The same experiments have been done for GS and LOC. Figure 17 illustrates the accuracy (in percentage) of DRFS architecture with the proposed AFC in various input levels. Regarding the sensitivity of these systems before and after integrating the AFC, the results indicate that the proposed AFC increases the sensitivity of LOC and GS by an amount of 26 and 8 dB respectively.

VHF Radio

In this test, IFR-4000 is set to AM COM mode, the output level is -80 dBm, creating the tone at 1020 Hz. The signal of each tuning word (no correction, manual tuning, and AFC correction) is demodulated and are processed by MATLAB to calculate the Signal-to-Noise Ratio (SNR), Total Harmonic Distortion (THD) and Signal-to-Noise and Distortion ratio (SINAD). The result, as summarized in Table 3 shows that the signal of the AFC has the best performance for all three parameters.

### Table 3. Performance Result of VHF Radio Before/After Using AFC

<table>
<thead>
<tr>
<th>Tuning word</th>
<th>SNR (dB)</th>
<th>THD (dB)</th>
<th>SINAD (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>No tuning</td>
<td>0.54</td>
<td>-21.77</td>
<td>0.51</td>
</tr>
<tr>
<td>Manual Tuning</td>
<td>8.72</td>
<td>-40.61</td>
<td>8.72</td>
</tr>
<tr>
<td>AFC Correction</td>
<td>9.06</td>
<td>-42.55</td>
<td>9.05</td>
</tr>
</tbody>
</table>

**Conclusion and Perspectives**

Table 4 summarizes the sensitivity of the DRFS architecture before applying the proposed AFC (non-corrected and manual corrected tuning word) and after the implementation. It is clear that the integration of the proposed FFT based AFC improves the performance of each system by correcting the roundup and quantization of the tuning word. In addition, it offers the possibility to track the signal that has an offset from the assigned frequency. With the integration of this module, the DRFS architecture meets the required sensitivity for GS, and it is lower than LOC and VOR standards only by 8 and 3 dB, without any analog supports such as Low Noise Amplifier (LNA) and filters. Implementation of this RF Front-End is the next step of the research, in order to be capable of testing the DRFS architecture in a flight test.

Even though the required resource in FPGA to integrate this system might be variable depending on FFT length, filters, etc. the implementation of a configurable and controllable system reduced the number of the AFC from one AFC per SOI to one AFC for all SOIs, hence saving LUTs and registers. It
is true that the approach for the AFC presented in this paper has some limitations, in particular the incompatibility with FM signals. Nevertheless, in the scope of the SOIs and the avionic applications in general, it can adapt the requirements for both sensitivity and dynamic range. An interesting subject for further developments will be reducing the latency of tracking time, so the utilization of this module could be expanded for pulse and message signals in VHF band, for examples, VHF Data Link Broadcast (VDB) and Aircraft Communication and Reporting System (ACARS).

**Table 4. Performance Result Summaries**

<table>
<thead>
<tr>
<th>Standard (dBm)</th>
<th>DRFS (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>No AFC</td>
</tr>
<tr>
<td>VOR</td>
<td>-93</td>
</tr>
<tr>
<td>GS</td>
<td>-77</td>
</tr>
<tr>
<td>LOC</td>
<td>-87</td>
</tr>
</tbody>
</table>

**References**


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